Drain Current Models for Single-Gate Mosfets & Undoped Symmetric & Asymmetric Double-Gate SOI Mosfets And Quantum Mechanical Effects: A Review

SUBHA SUBRAMANIAM
PhD Student, Department of Electrical Engineering, VJTI Matunga, Mumbai-19, INDIA subha.sakec@gmail.com

R.N.AWALE
PROFESSOR, Department of Electrical Engineering, VJTI Matunga, Mumbai-19, INDIA rnavale@vjti.org.in

SANGEETA M.JOSHI
PRINCIPAL, Smt. Indira Gandhi College of Engineering Navi Mumbai, INDIA sangeetamjoshi@gmail.com

Abstract:
In this paper modeling framework for single gate conventional planar MOSFET and double gate (DG) MOSFETS are reviewed. MOS Modeling can be done by either analytical modeling or compact modeling. Single gate MOSFET technology has been the choice of mainstream digital circuits for VLSI as well as for other high frequency application in the low GHZ range. The major single gate MOS modeling methods are reviewed and compared. First generation to fifth generation MOS models like BSIM & PSP are compared. The use of multiple gates has emerged as a new technology to replace the conventional planar MOSFET when its feature size is scaled to the sub 22nm regime. Double Gate devices seem to be attractive alternatives as they can effectively reduce the short channel effects and yield higher current drive. DGFETS are classified as Symmetric Double Gate FETs (SDGFET) and Asymmetric Double Gate FETs (ADGFET). This paper covers the fundamentals of SDGFETs and ADGFETs. Drain current models for single gate MOSFETs, SDGFETs and ADGFETs are reviewed. In the Double gate MOS era the dominating quantum mechanical effects which has to be considered in two dimensional modeling are also discussed. The comparisons of drain current models for Symmetric and Asymmetric Double gate MOSFETs are done and shown with the results like limitations of the models. A brief summary of the review work is provided. The result shows a greater demand in the field of Asymmetric Double gate modeling which can be extended for circuits like SRAM and RF amplifier design. The premier quantum mechanical effects which should be included in model development for below 22nm devices are listed.

Keywords: Double Gate MOSFET (DGFETs), MOS Modeling, Analytical modeling, Compact Modeling, Drain current model.

1. INTRODUCTION
Silicon-based microelectronic devices have revolutionized our world in the past four decades. The need for higher computing power at cheaper cost has fueled incessant CMOS scaling. It all started with the invention of integrated circuit in late 1950’s that unveiled the possibility of using transistors in almost all kinds of electronic circuits. The next major breakthrough came with the demonstration of the first metal-oxide semiconductor field-effect transistor (MOSFET) in 1960 by Kahng and Atalla which would enable cost-effective integration of large number of transistors with interconnections on a single silicon chip. Five years later, Gordon Moore made the very important observation that the number of components on minimum cost integrated circuits had increased roughly by a factor of two per year which then later transformed itself into a law known as the Moore’s Law[2]. Moore’s Law is achieved primarily by scaling the transistor dimensions by a factor of 2 every 3 years. CMOS devices have been scaled down aggressively in each technology generations to achieve higher integration density and performance [3]. The leakage current has increased drastically with technology scaling and has become a major contributor to the total IC power [4]. As the down scaling includes many short channel and quantum mechanical effects, MOS modeling becomes a great challenge in the semiconductor industry to predict the device characteristics accurately by the simulators.
1.1. Modeling

Models form a bridge between the design world and the manufacturing world. Accurate models describe the behavior of the transistors in the circuit which is used by the simulators. Modeling is essential to simulate the operation of integrated circuit (IC) before its fabrication. The circuit designer’s efficiency to develop a circuit depends mainly on the device model. The accuracy and simplicity of the model has a deep influence on the designing and fabrication of the circuit. Thus device models act as a bridge between the integrated circuit designers and those working for process technology development as shown in Fig. 1. Any device model is categorized as numerical models and compact models. Numerical models are based on solving the partial differential equations (PDE) describing the detailed physics of the device. These models are computationally intensive, complex and take a lot of computation time to solve the circuits. However, compact models treats the device as a black box and simple closed form expressions for terminal current, voltage, capacitance and charges are derived. It describes the device in a simplified manner and also they are fast. (e.g.) BSIM, PSP, EKV [7].

Fig 1. Complete Flow of the Technology, Modeling and Design

2. MOS Modeling

Analytical or semi analytical MOSFET models are usually based on the gradual channel approximation (GCA). Contrary to the situation in the ideal two-terminal MOS device, where the charge density profile is determined from a one-dimensional Poisson’s equation, the MOSFET generally poses a two-dimensional electrostatic problem. The reason is that the geometric effects and the application of a drain-source bias creates a lateral electric field component in the channel, perpendicular to the vertical field associated with the ideal gate structure. The GCA (gradual channel approximation) states that, under certain conditions, the electrostatic problem of the gate region can be expressed in terms of two coupled one-dimensional equations – a Poisson’s equation for determining the vertical charge density profile under the gate and a charge transport equation for the channel. This allows us to determine self-consistently both the channel potential and the charge profile at any position along the gate. A direct inspection of the two-dimensional Poisson’s equation for the channel region shows that the GCA is valid if we can assume that the electric field gradient in the lateral direction of the channel is much less than that in the vertical direction perpendicular to the channel (Lee et al. 1993). Typically, we find that the GCA is valid for long-channel MOSFETs, where the ratio between the gate length and the vertical distance of the space charge region from the gate electrode, the so-called aspect ratio, is large. However, if the MOSFET is biased in saturation, the GCA always becomes invalid near drain as a result of the large lateral field gradient that develops in this region. Three relatively simple MOSFET models, the simple charge control model, the Meyer model, and the velocity saturation model are known as the first generation models [8].

2.1 Simple Charge Control Model (SCCM)

This model assumes a long n channel MOSFET operating in the above threshold regime with a gate voltage sufficiently high to cause inversion in the entire length of the channel at zero drain source bias. The basic assumptions are GCA is applicable and the carrier mobility taken to be constant and no velocity saturation included. The model proves that the threshold voltage decreases with decreasing insulator thickness and is quite sensitive to substrate bias. This so-called body effect is essential for device characterization and in threshold voltage engineering.

\[ V_{SAT} = V_{GT}, \text{ Assuming a constant electron mobility} \] [8]

\[ I_{ds} = W \mu_n q n_x F, \]

\[ I_{ds} = \frac{W \mu_n q n_x F}{L} \times \begin{cases} (V_{GT} - V_{DS}/2)V_{DS}, & \text{for } V_{DS} \leq V_{SAT} = V_{GT} \\ V_{GT}^2/2, & \text{for } V_{DS} > V_{SAT} \end{cases} \]
2.2 Meyer Model (MM)
The Meyer model, the lateral variation of the depletion charge in the channel is taken into account. This model accounts the total induced charge $q_s$ per unit area in the semiconductor n channel MOS including both inversion and depletion charges and express it in terms of Gauss’s law. Assuming source and semiconductor substrate are both connected to ground [9]

$$q_s = -c_i [V_{GS} - V_{FB} - 2\varphi_b - V(x)].$$

$$I_{ds} = W \mu_n q_n(x) F(x),$$

$$I_{ds} = \frac{W \mu_n c_i}{L} \left\{ \left( V_{GS} - V_{FB} - 2\varphi_b - \frac{V_{DS}}{2} \right) V_{DS} - \frac{2\sqrt{2\varepsilon_s q_n N_A}}{3c_i} \left( V_{DS} + 2\varphi_b \right)^{3/2} - \left( 2\varphi_b \right)^{3/2} \right\}.$$ 

At low doping levels it is proved that $V_{sat}$ is approximately equal to $V_{GT}$, which is same as the result found for SCCM.

2.3 Velocity Saturation Model (VSM)
The linear velocity-field relationship (constant mobility) used in the above MOSFET models works reasonably well for long-channel devices. However, the implicit notion of a diverging carrier velocity as we approach pinch-off is, of course, unphysical. Instead, current saturation is better described in terms of a saturation of the carrier drift velocity when the electric field near drain becomes sufficiently high. This two-piece model shows the velocity-field relationship:

$$v(F) = \begin{cases} \mu_n F & \text{for } F < F_s \\ v_s & \text{for } F \geq F_s. \end{cases}$$

where $F = |dV(x)/dx|$ is the magnitude of lateral electrical field in the channel, $V_s$ is the saturation velocity, and $F_s = V_S / \mu n$ is the saturation field. In this description, current saturation in FETs occurs when the field at the drain side of the gate reaches the saturation field[10].

$$I_{ds} = \frac{W \mu_n c_i}{L} \times \begin{cases} V_{GT} V_{DS} - V_{DS}^2 / 2, & \text{for } V_{DS} \leq V_{SAT} \\ (V_{GT} - V_{SAT}) V_L, & \text{for } V_{DS} > V_{SAT}. \end{cases}$$

$$V_{SAT} = V_{GT} - V_L \left[ \sqrt{1 + (V_{GT} / V_L)^2} - 1 \right].$$

2.5 Comparison of Basic MOSFET Models
The I–V characteristics shown in Fig 2 were calculated using the three basic MOSFET models - the simple charge control model (SCCM), the Meyer I–V model (MM), and the velocity saturation model (VSM). The same set of MOSFET parameters were used in all cases. Mostly all models coincide at small drain-source voltages. However, in saturation, SCCM always gives the highest current. This is a direct consequence of omitting velocity saturation and spatial variation in the depletion charge in SCCM, resulting in an overestimation of both carrier velocity and inversion charge. The characteristics for VSM and MM clearly demonstrate how inclusion of velocity saturation and distribution of depletion charge, respectively, affect the saturation current. Therefore, we emphasize that SCCM is usually applicable only for long-channel, low-doped devices, while MM applies to long-channel devices with an arbitrary doping level. VSM gives a reasonable description of short-channel devices, although important short-channel effects such as channel-length modulation and drain-induced barrier lowering (DIBL) are still unaccounted for in these models [8].
2.6 Review of BSIM Models

The SCCM, Meyer and VSM models with extensions are used as the SPICE models Level 1, Level 2, Level 3 are called first generation SPICE Models. Level 1 model is used for gate lengths greater than 5 um. Level 2 model (gate length < 5 um) is much more complex than Level 1 model. It includes mobility reduction due to high gate fields, threshold voltage reduction due to charge sharing in the channel and velocity saturation. Level 3 model (gate length < 1 um) is more empirical in nature. The second generation models viz. BSIM1, HSPICE level 28, BSIM2 are used for sub-half micron lengths. They have separate parameters for geometry dependence which are fitted with the parameters extracted for a particular dimension. The third generation of charge based models is the advanced versions of the BSIM models. These are BSIM3, BSIM4 and BSIM5. These models are for deep sub-micron and nanometer scale MOSFETs. More physical effects have been taken in this model, such as, the inclusion of quantum behavior of the MOSFET like quantization of inversion layers empirically, quantum mechanical charge-layer-thickness model for both I-V and C-V characteristics. This model also includes the accurate gate direct tunneling model. BSIM 5 is used for sub-100 nm CMOS circuit simulation [7].

2.7 Review of PSP Model (Pennsylvania State University)

PSP is the latest and most advanced compact model developed for short channel MOSFETs below sub-100nm by merging the best features of the two models Surface Potential based model (SP-developed at the Pennsylvania University) and Mobility Model (MM11-developed by Philips research). PSP Model provides physical & accurate description of accumulation region, complete Gummel Symmetry, Quantum Mechanical Corrections, Correction for polysilicon depletion effects, Solution for GIDL (Gate Induced Drain Leakage) & GISL (Gate Induced Source Leakage).

3. Double Gate MOSFET (DGFET)

The technology beyond 45nm has switched to different device structures and Double Gate FET (DGFET) predominates the industry because of the better control over channel by two gates[1]. Modeling DGFETs with two gate structure is a great challenge. This section covers the fundamentals of DGFETs. The schematic of a generic n-channel DGFET is shown in Fig.3. The shaded region is the gate dielectric (and spacer). $t_{of}$ and $t_{ob}$ are the thicknesses of the front and back gate dielectrics. In a DGFET the channel is under the control of two gates, viz. the front and back gates. This helps in reducing the effect of the drain field in reaching the source, and thus results in reduced short channel effects (SCE). A DGFET with identical material and thickness for the front and back gate electrodes and dielectric is called a symmetric DGFET (SDGFET).
3.1 Fundamentals of SDGFETs
The symmetric double gate device’s two oxide thicknesses are equal, the two gates have the same flatband voltage, [12] and the gates are connected together. The main parameters of symmetric DG SOI MOSFETs are electrostatic potential and drain–current.

3.2 Energy Band Diagram of SDGFET
Energy band diagrams across the channel at two gate biases for symmetric DGFETs are shown in Fig. 4. In a SDGFET with a mid-gap gate electrode, the bands in silicon are flat in the sub-threshold regime, implying a uniform (and low) carrier density across the fin. At high gate bias, the bands in silicon bend downwards near the sidewalls. When they are sufficiently bent so as to be near or above the quasi Fermi level (which is spatially flat along the fin at VDS=0), the carrier density near the sidewalls increases sharply, and the transistor is said to be strongly inverted. There are various definitions for the exact onset of strong inversion. [14] The gate bias corresponding to the onset of strong inversion is called the threshold voltage $V_t$

3.3 Description of Potential of SDGFET
Considering the case that the contribution of holes is negligible and the electrostatic potentials $\psi = kT/e$, the solution of the one-dimensional Poisson equation in the x direction of the channel region, under the quasi-equilibrium approximation, leads to the following two equations [13]

$$V_G = \psi_S + \frac{\sqrt{2kTn_i^2e_s}}{C_o} \sqrt{e^{-\beta V} (e^{\beta \psi_S} - e^{\beta \psi_S})} \tag{1}$$

and

$$\psi_S = \psi_S - \frac{2}{\beta} \ln \left\{ \cos \left\{ \frac{q^2n_i e_s (\psi_S - \psi_S)}{2kT} \right\} \right\} \tag{2}$$

where $V_G$ is the difference between the applied gate-to-source voltage and the flatband voltage, $\beta = e/kT$ is the inverse of the thermal voltage, $n_i$ is the intrinsic free carrier density, $\psi_S$ is electrostatic potential at the surface ($x = t_{Si}/2$), $\psi_S$ is the potential extremum at the center of the silicon film ($x = 0$), $C_o$ is the gate oxide capacitance per unit area, $e_s$ is the permittivity of the semiconductor, $t_{Si}$ is the semiconductor film thickness, and $V$ is the potential difference between electron and hole quasi-Fermi levels along the channel (i.e., voltage drop in the channel), which is equal to zero at the source and $V_{DS}$ at the drain.

3.4 Double Integral Formulation for Drain Current:
The drain–current can be described following the idea of Pao & Sah [11] that includes both the drift and diffusion transport tendencies in the silicon film, resulting in a current description with smooth transitions between the linear and saturation operating regions[21],[22]. Under the approximation that the mobility is independent of the position in the channel, the drain–current

$$I_D = \mu \frac{W}{L} \int_{0}^{V_{DS}} Q_I \, dV \tag{3}$$

where $Q_I$ is the total (integrated in the transverse direction) inversion charge density inside the silicon film of a symmetric DGFET at a given location y,
3.5 Surface potential based Models

Two surface potential-based models by Ortiz-Conde et al and Taur et al. have been reported. Ortiz-Conde Model followed the double integral equation of bulk MOS Devices and transformed it for DG-SOI devices without any approximations. Taur et al. Model introduced a new auxiliary variable $\beta T$ into the double integral and solved for drain current. Both the models result in same drain current expression with the substitution of $\beta T[17]$. 

3.6 Charge Based Models

Since there is no depletion charge in an intrinsic material, the inversion charge is equal to the total charge in the undoped channel. It allows for the correlation between the inversion charge and the surface potential. Two charge-based models are proposed by He et al and Sallese et al[20]. He et al. proposed a drain current equation based on charges and it is not equivalent to the surface potential models. Sallese et al developed an expression for drain current which is showing equivalent result with numerical models is shown in Fig 6.

![Fig 6. Comparison of charge based drain current models of He’s and Sallese’s models.](image)

Table 1. Comparison of Drain Current Models-SDGFETs

<table>
<thead>
<tr>
<th>Sr.No</th>
<th>Author’s Name</th>
<th>Basic Modeling Methods</th>
<th>Limitations</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>Dunga. et al</td>
<td>Charge sheet approximation using perturbation technique(BSIM-CMG)[21],[22]</td>
<td>Only above threshold region &amp; constant mobility</td>
</tr>
<tr>
<td>02</td>
<td>Taur’s Group</td>
<td>one dimensional single piece model [16]</td>
<td>Constant mobility</td>
</tr>
<tr>
<td>03</td>
<td>He.et.al</td>
<td>One dimensional inversion charge based model using Lambert-W function,[18]</td>
<td>No closed form solution of Lambert-W function.</td>
</tr>
<tr>
<td>04</td>
<td>EKV Group</td>
<td>one dimensional inversion charge based model using implicit equation.</td>
<td>Constant mobility &amp; approximation in calculation of inversion charge areal density</td>
</tr>
<tr>
<td>05</td>
<td>Wong Shi</td>
<td>Inversion charge based model including mobility degradation &amp; velocity saturation [19]</td>
<td>One effect turned at a time for simplicity.</td>
</tr>
<tr>
<td>06</td>
<td>Sodini Ko Moll</td>
<td>Caughty thomas model</td>
<td>Violates gummel symmetry complaint</td>
</tr>
<tr>
<td>07</td>
<td>PSP Finfet model</td>
<td>One dimensional surface potential based model for finfets with temperature variations included. [32]</td>
<td>Constant mobility</td>
</tr>
</tbody>
</table>
3.8 SUMMARY of SDGFET Models

To summarize, a vast majority of the core models in the literature have been developed using constant mobility. The only core model [19] for an SDGFET that considered velocity saturation within the boundary of the core model, was not Gummel-symmetry compliant. It is thus clear from this review that there exists a need for a core model that goes beyond constant mobility considerations and in a manner that Gummel-symmetry is preserved. The greater the number of physical effects considered in the core model (as opposed to adding them as second order effects onto a constant mobility core model), the greater is the physical accuracy (and complexity) of the model.

4. Fundamentals of ADGFETs

The asymmetric double gate device’s two oxide thicknesses are not equal, the two gates have different flatband voltage [12] and two different gate biases. For the generalized case of Asymmetric devices, the electric field may not vanish inside the semiconductor film. Therefore, it is not convenient to select the origin of the x-axis at the center of the silicon. For this case, we select the origin of the x-axis at the front surface. Energy band diagrams across the channel at two gate biases for asymmetric DGFETs are shown in Fig. 7. In a ADGFET with a mid-gap gate electrode, the bands in silicon are not flat in the sub-threshold regime, implying a uniform (and low) carrier density across the fin. At high gate bias, the bands in silicon bend downwards near the sidewalls.

4.1 Drain Current for ADGFETs

Ortiz-Conde et al. followed the idea of Pierret and Shields for bulk MOS devices transformed the double integral equation and derived the drain current equation. This equation is valid for any Asymmetric condition as long as the electric field does not vanish inside the film.[21],[22],[22].

\[
I_D = \mu \frac{W}{L} \left( C_{ov} \left( V_{Gr} + \frac{2}{\beta} \right) (\psi_{dL} - \psi_{sto}) + \frac{1}{2} \left( \psi_{dL}^2 - \psi_{sto}^2 \right) + \frac{\varepsilon_{Si} f_{Si}}{2} (\alpha_o - \alpha_L) \right.
\]

\[
+ C_{ob} \left( V_{Gb} + \frac{2}{\beta} \right) (\psi_{aL} - \psi_{abo}) - \frac{1}{2} (\psi_{aL}^2 - \psi_{abo}^2) \]

\[
- n_k T e_{Si} (\beta V_D + \exp(-\beta V_D) - 1) \right) \]

Fig 7. Energy Band Diagram of ADGFETS
Table 2. Comparison of ADGFET Drain Current Models

<table>
<thead>
<tr>
<th>Sr.No</th>
<th>Author’s Name</th>
<th>Basic Modeling Methods</th>
<th>Limitations</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>Lu &amp; Taur</td>
<td>Different $V_{fb}$ flatband voltage[21],[22]</td>
<td>Only Numerical solution</td>
</tr>
<tr>
<td>02</td>
<td>Roy</td>
<td>Different regional expression via interpolation function [21],[22]</td>
<td>No velocity saturation</td>
</tr>
<tr>
<td>03</td>
<td>Pei et.al</td>
<td>One dimensional $V_{th}$ based closed form model using caught Thomas model.</td>
<td>Above threshold region is only modeled</td>
</tr>
<tr>
<td>04</td>
<td>EKV group</td>
<td>Common and differential mode gate voltage</td>
<td>No velocity saturation</td>
</tr>
<tr>
<td>05</td>
<td>Taur’s Group</td>
<td>Ward-Dutton Charge part Look-up table method[16]</td>
<td>Assuming constant charge</td>
</tr>
<tr>
<td>06</td>
<td>Zhu et.al</td>
<td>Surface potential based model using lambert-w function</td>
<td>Assuming mobility Constant mobility</td>
</tr>
</tbody>
</table>

4.4 SUMMARY of ADGFET Models:
As per the review very less people have worked on ADGFET models. Most of the models are derived from SDGFETs only. In reality ADGFET physics is more complex than SDGFETs. But the asymmetry of gates can be used in applications like SRAM and RF amplifiers to reduce the power and increase the gain. More compact models should be developed in Asymmetric DGFETs so that it can be applied to design low power circuits.

5. Quantum Mechanical Effects in DGFETs

5.1 Gate Induced Drain Leakage (GIDL)
Minimization of transistor off-state leakage current is an especially important issue for low-power circuit applications. A large component of off-state leakage current is gate induced drain leakage (GIDL) current, caused by band-to-band tunneling in the drain region underneath the gate when there is a large gate-to-drain bias, there can be sufficient energy-band bending near the interface between silicon and the gate dielectric for valence-band electrons to tunnel into the conduction band. GIDL imposes a constraint for gate-oxide thickness scaling because the voltage required to cause this band-to-band tunneling leakage current decreases with decreasing gate oxide thickness, and GIDL can pose a lower limit for standby power in memory devices.[31]

5.2 Quantum Mechanical Tunneling from source to gate oxide
Due to aggressive technology scaling, the gate oxide thickness will be only around 2 nm in nanometer scale devices and thus called as ultra thin oxides. In the ultra thin oxide MOSFETs, the electrical field will be very high. Hence, the charge carriers in the channel will directly tunnel through the interface barrier to the gate oxide [33],[34],[35].

5.3 Energy quantization in the substrate
As the MOSFET dimensions approach deep submicron and nanometer regions, the classical movement of the charge carriers is greatly affected by the nonclassical behavior of electrons in the MOSFET. Due to aggressive scaling of the MOSFETs, the gate oxides are also scaled to nanometer regions. Also, the substrate doping is increased tremendously to negate the short channel effects at the deep sub-micrometer or nanometer scales. This results in very high electric fields in the silicon/silicon oxide interface and hence the potential at the interface becomes steeper. This results in a potential well between the oxide field and the silicon potentials. During the inversion condition, the electrons are confined in this potential well [33],[34],[35]. Due to confinement, the electron energies are quantized and hence the electrons occupy only the discrete energy levels. Due to Energy Quantization, charge carrier density at the surface becomes less than the one expected from the classical analysis.

5.4 Quantum tunneling from source to drain in the substrate
In sub 10nm channel length, the charge carriers are no longer restricted in the source potential well but start tunnelling quantum mechanically through the barrier between the source and drain [33],[34],[35]. So, the gate voltage has no control over the MOSFET operation. This process is very important to model so as to continue with the scaling down process beyond 10 nm gate lengths.
5.5 Threshold voltage and drain saturation voltage shift

The shift in the surface potential due to the quantum mechanical effects changes the threshold voltage as the effective oxide thickness increases. [33],[34],[35].

6. Conclusion

In DGFET modeling the new and accurate techniques should be developed to analyze the device behavior under various biasing and different temperature variations. Quantum mechanical effects like tunneling from source to gate oxide and source to drain, energy quantization and threshold voltage shift should be considered in DGFETs and the new two dimensional models should be developed which can characterize the devices with these effects in the simulators. The device can be modeled according to the customer need and for particular applications like memories (SRAM) and RF Designs. This work can be extended further for FINFET modeling to get better accuracy in device simulators. The economics behind the CMOS scaling is strong enough to keep it alive for several more generations to come. Multi-Gate transistors present an interesting alternative to extend the CMOS scaling. But at the same time, the conventional planar bulk silicon MOSFET continues to shrink aided by incorporation of new materials into the conventional MOSFET structure, be it the gate-dielectric or the gate electrode or the source/drain region. New compact models will continue to emerge alongside new FET architectures to enable evaluation of these new architectures. At the same time, the existing models for bulk FETs will continue to incorporate new physics to describe advanced bulk FETs.

Nanoscale CMOS is an endless exciting road for both technology and model developers.

7. REFERENCES

[21] Adelmo Ortiz-Conde, Senior Member, IEEE, Francisco J. Garcia-Sanchez, Senior Member, IEEE, Juan Mucci,Slavica Malobabic, Student Member, IEEE, and Juin J. Liou, Senior Member, IEEE. "A Review of Core Compact Models for Undoped Double-Gate SOI MOSFETs," IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 54, NO. 1, JANUARY 2007
[22] Jooyoung Song, Student Member, IEEE, BoYu, Student Member, IEEE, Yu Yuan, and Yuan Taur, Fellow, IEEE. "A Review on Compact Modeling of Multiple-Gate MOSFETs," IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, VOL. 56, NO. 8, AUGUST 2009


[29] Venkatnarayan Hariharan, Student Member, IEEE, Juzer Vasi, Fellow, IEEE, and V. Rangopal Rao, Senior Member, IEEE, "Drain Current Model Including Velocity Saturation for Symmetric Double-Gate MOSFETs," 10.1109/TED.2008.926745.


